UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/819,883	03/28/2001	Finbarr Denis Long	SRT-022	1043

21323 7590 07/21/2004

TESTA, HURWITZ & THIBEAULT, LLP
HIGH STREET TOWER
125 HIGH STREET
BOSTON, MA 02110

EXAMINER	
MANOSKEY, JOSEPH D	

ART UNIT	PAPER NUMBER
2113	9

DATE MAILED: 07/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/819,883	Applicant(s) LONG ET AL.	
	Examiner Joseph Manoskey	Art Unit 2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7-15 and 19-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-15 and 19-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/2/03 & 5/3/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 24 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 24 recites the limitation "the packets" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 1-3, 7-15, and 19-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thorson et al., U.S. Patent 6,643,764, hereinafter referred to as "Thorson", in view of Rostoker et al., U.S. Patent 5,446,726, hereinafter referred to as

"Rostoker", and Fletcher et al., U.S. Patent 3,783,250, hereinafter referred to as "Fletcher".

6. Referring to claim 1, Thorson teaches a plurality of data processing elements (See Fig. 2). Thorson also teaches a router containing a lookup table that is associated with interface ports, that include processor interface ports and I/O interface ports, which is interpreted as an I/O node in communication with at least one of the plurality of data processing elements (See Col. 3, lines 44-57). Finally, Thorson discloses a router for transferring communications between nodes (See Fig. 2). This is interpreted as a switching fabric communicating transactions between at least one of the plurality of data processing elements and the I/O node.

Thorson does not teach the data processing elements executing substantially identical instruction streams substantially simultaneously or the switching fabric communicating transactions asynchronously, however Thorson does show a desire to increase bandwidth to increase over all performance (See Col. 1, lines 35-41) and a desire to increase the fault tolerance of the infrastructure (See Col. 1, lines 42-50).

Rostoker teaches the use of an ATM (asynchronous transfer mode) protocol integrated with a router in a network (See Fig. 1). Fletcher discloses a plurality of processors redundantly running the same operation (See Col. 1, lines 58-66).

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the ATM protocol of Rostoker with the router of Thorson and the redundant processors of Fletcher with plurality of processors of Rostoker. This would have been

obvious to one of ordinary skill in the art at the time of the invention to do because the ATM protocol is highly advantageous in that it enables high speed transmissions (See Rostoker, Col. 2, lines 22-25), thus allowing higher bandwidth, and the redundant processors allow continued operation in the event of a failure (See Fletcher, Col. 2, lines 22-26).

7. Referring to claim 2, Thorson, Rostoker, and Fletcher disclose all the limitations (See rejection of claim 1), including the processors redundantly running the same operation (See Col. 1, lines 58-66). This is interpreted as the data processing elements execute the same instruction in lock-step synchronization.

8. Referring to claims 3 and 4, Thorson, Rostoker, and Fletcher teach all the limitations (See rejection of claim 1), including the plurality of data processing elements comprising a central processing unit and wherein the CPU further comprises a plurality of processors (See Rostoker, Fig. 1 and 2).

9. Referring to claims 7 and 8, Thorson, Rostoker, and Fletcher disclose all the limitations (See rejection of claim 1), including the nodes being connected to the router via an interface chip (See Rostoker, Fig. 2). This is interpreted as a channel adapter interconnects the I/O node to the switching fabric and a plurality of channel adapters interconnect respectively, each of the plurality of data processing elements to the switching fabric.

10. Referring to claim 9, Thorson, Rostoker, and Fletcher teach all the limitations (See rejection of claim 1), including the use of triple buffer registers in the voter-comparator-switch (See Fletcher, Fig. 3). This is interpreted as a plurality of voter delay buffers, wherein each of the plurality of voter delay buffers is in communication with at least one of the plurality of data processing elements.

11. Referring to claim 10, Thorson, Rostoker, and Fletcher disclose all the limitations (See rejection of claim 1), including the ATM unit including a DMA for interconnecting to a host unit (See Rostoker, Col. 3, lines 29-31), which is interpreted as a plurality of direct memory access engines in communication with the switching fabric.

12. Referring to claims 11 and 12, Thorson, Rostoker, and Fletcher teach all the limitations (See rejection of claim 1), including the router using a lookup table to determine destination addresses (See Thorson, Fig. 2 and 4). This is interpreted as the data processing elements being identified by a node address which is a respective device address.

13. Referring to claim 13, Thorson, Rostoker, and Fletcher disclose all the limitations (See rejection of claim 1), including the routing of packets in the multiprocessor system (See Thorson, Col. 4, lines 1-2), which is interpreted as the transaction comprising at least one information packet.

14. Referring to claim 14, Thorson teaches a plurality of data processing elements (See Fig. 2). Thorson also teaches a router containing a lookup table, which is used to determine a destination address, that is associated with interface ports, that include processor interface ports and I/O interface ports, which is interpreted as communicating transactions on a switching fabric to the I/O node identified by the I/O node address (See Fig. 2 and 4, Col. 3, lines 44-57).

Thorson does not teach the data processing elements executing identical instruction streams substantially simultaneously or the switching fabric communicating transactions asynchronously, however Thorson does show a desire to increase bandwidth to increase over all performance (See Col. 1, lines 35-41) and a desire to increase the fault tolerance of the infrastructure (See Col. 1, lines 42-50).

Rostoker teaches the use of an ATM (asynchronous transfer mode) protocol integrated with a router in a network (See Fig. 1). Fletcher discloses a plurality of processors redundantly running the same operation (See Col. 1, lines 58-66).

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the ATM protocol of Rostoker with the router of Thorson and the redundant processors of Fletcher with plurality of processors of Rostoker. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because the ATM protocol is highly advantageous in that it enables high speed transmissions (See Rostoker, Col. 2, lines 22-25), thus allowing higher bandwidth, and the redundant

processors allow continued operation in the event of a failure (See Fletcher, Col. 2, lines 22-26).

15. Referring to claim 15, Thorson, Rostoker, and Fletcher disclose all the limitations (See rejection of claim 14), including receiving incoming commands from the computer modules to the IOP/voter-comparator-switch which selects the output (See Fletcher, Fig. 1 and 3). This is interpreted as communicating identical transactions to a voting unit and transmitting by the voting unit a single transaction asynchronously on the a switching fabric.

16. Referring to claim 19, Thorson, Rostoker, and Fletcher teach all the limitations (See rejection of claim 14), including the nodes being connected to the router via an interface chip (See Rostoker, Fig. 2). This is interpreted as communicating each of the identical transactions of the data processing elements to the channel adapter, from the channel adapter to the router, then from the router to the next channel adapter, and finally communicating the transaction from the channel adapter to the I/O node.

17. Referring to claim 20, Thorson teaches a plurality of data processing elements (See Fig. 2). Thorson also teaches a router containing a lookup table that is associated with interface ports, that include processor interface ports and I/O interface ports, which is interpreted as an I/O node in communication with at least one of the plurality of data processing elements (See Col. 3, lines 44-57). Finally, Thorson discloses a router for

transferring communications between nodes (See Fig. 2). This is interpreted as a switching fabric communicating transactions between at least one of the plurality of data processing elements and the I/O node.

Thorson does not teach the data processing elements executing substantially identical instruction streams substantially simultaneously, a voting module in communication with the data processing elements for comparing the I/O instructions associated with two of the plurality of data processing elements or the switching fabric communicating transactions asynchronously, however Thorson does show a desire to increase bandwidth to increase over all performance (See Col. 1, lines 35-41) and a desire to increase the fault tolerance of the infrastructure (See Col. 1, lines 42-50).

Rostoker teaches the use of an ATM (asynchronous transfer mode) protocol integrated with a router in a network (See Fig. 1). Fletcher discloses a plurality of processors redundantly running the same operation (See Col. 1, lines 58-66). Fletcher also teaches receiving incoming commands from the computer modules to the IOP/voter-comparator-switch which selects the output (See Fletcher, Fig. 1 and 3). This is interpreted as a voting module in communication with the data processing elements for comparing I/O instructions associated with at least two of the plurality of data processing elements.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the ATM protocol of Rostoker with the router of Thorson and the redundant processors of Fletcher with plurality of processors of Rostoker. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because the

ATM protocol is highly advantageous in that it enables high speed transmissions (See Rostoker, Col. 2, lines 22-25), thus allowing higher bandwidth, and the redundant processors allow continued operation in the event of a failure (See Fletcher, Col. 2, lines 22-26).

18. Referring to claim 21, Thorson, Rostoker, and Fletcher disclose all the limitations (See rejection of claim 20), including the processors redundantly running the same operation (See Col. 1, lines 58-66). This is interpreted as the data processing elements execute the same instruction in lock-step synchronization.

19. Referring to claims 22 and 23, Thorson, Rostoker, and Fletcher disclose all the limitations (See rejection of claim 20), including the nodes being connected to the router via an interface chip (See Rostoker, Fig. 2). This is interpreted as a channel adapter interconnects the I/O node to the switching fabric and at least one channel adapter interconnects the voting module and the switching fabric.

20. Referring to claim 24, Thorson, Rostoker, and Fletcher disclose all the limitations (See rejection of claim 20), including the nodes being connected to the router via an interface chip (See Rostoker, Fig. 2). This is interpreted as a plurality of channel adapters interconnect respectively, each of the plurality of data processing elements to the voting module and wherein the voting module compares the packets being

communicated from the channel adapters associated with at least two of the plurality of data processing elements.

21. Referring to claim 25, Thorson, Rostoker, and Fletcher teach all the limitations (See rejection of claim 20), including the use of triple buffer registers in the voter-comparator-switch (See Fletcher, Fig. 3). This is interpreted as a plurality of voter delay buffers, wherein each of the plurality of voter delay buffers is in communication with at least one of the plurality of data processing elements.

22. Referring to claim 26, Thorson, Rostoker, and Fletcher disclose all the limitations (See rejection of claim 20), including the routing of packets in the multiprocessor system (See Thorson, Col. 4, lines 1-2), which is interpreted as the transaction comprising at least one information packet.

Response to Arguments

23. All corrections to the specification and drawings, see Amendment A, filed 3 May 2004, have been entered and therefore the objections have been withdrawn.

24. Applicant's arguments, see Amendment A, filed 3 May 2004, with respect to the rejection(s)of claim(s) 1-3, 8, 11, 12, 14, and 19 under 35 U.S.C. 102 and claims 4, 7, 9, 10, 13, and 15 under 35 U.S.C. 103 have been fully considered and are persuasive.

Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of the above cited prior art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Manoskey whose telephone number is (703) 308-5466. The examiner can normally be reached on Mon.-Fri. (8am to 4:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JDM
July 13, 2004

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100